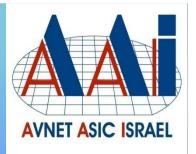
Over 20 Years Providing
Complete ASIC & COT Solutions

AAI company Presentation

www.avnet-asic.com

This presentation contains confidential information and cannot be forwarded to any third party without prior written approval from AAI

AAI Positioning



AAI is a World Class ASIC Design and manufacturing House (as quoted by our customers and suppliers)

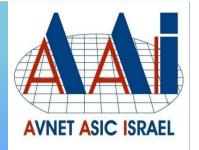
AAI is Number One ASIC Design Center in Israel, serving fabless & OEM companies in Israel and Worldwide

AAI is a subsidiary of Avnet Inc. (largest electronics distributor in the world)
AAI is a stable and profitable company, serving customers for over 20 years in an extremely demanding and volatile market.

AAI has established cooperation agreements with the world's leading ("Tier 1") Silicon, IP, CAD, Assembly and Test vendors

AAI is a "One Stop Shop" for ASIC design and implementation (Spec to RTL to GDSII, Analog Design, Structured ASIC, Transfer to Production and Manufacturing)

AAI Mission



To maintain high quality design standards and business ethics while securing first-time-siliconsuccess at fast time-to-market and time-to-production

To identify and execute key ASIC & COT programs and provide custom solutions and flexible services for all phases of the design cycle to fabless companies and OEMs

To provide our customers flexible business models and interface points to best fit their application requirements and their capabilities

To supply our customers with complete design and T/K manufacturing solutions, i.e. RTL logic design, RTL to GDSII, assembly/test and devices supply

Core Business



ASIC/SoC Design and Implementation: Logic Design IP Integration RTL to GDSII Flow (Synthesis, Layout, Formal, DFT, etc.) Transfer to production and manufacturing services Test and Package Development Quality and Reliability Production Logistics Management Design Conversions: **FPGA** → ASIC - for lower cost and power and higher performance **SASIC** → ASIC – pin compatible solutions for performance upgrade (power and frequency), cost reduction, End of Life, manufacturing transition. Custom Analog - Design and Production





Custom solutions (no available off-the-shelf devices)

Create Proprietary Systems (ASIC is unique)

Long Product Life (not depending on device suppliers)

Cost Reduction for Mass Production (System-on-Chip)

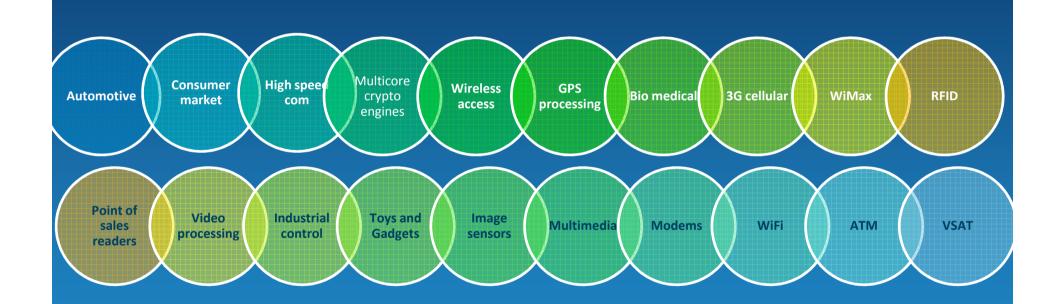
Improve Performance, Less Power, Less PCB area (better reliability)

FPGA → ASIC Conversions in Mass Production

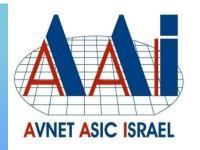
ASIC → **ASIC** Conversion (EOL, performance upgrade, features)

Experience in markets and applications





AAI Proven path to silicon - Some examples.



FIRST
WiMAX chip
in the world,
90nm NXP.

FIRST multi-core Cryptoengine chip, first design at Europe 65nm Fujitsu. FIRST
MDTV receiver chip
with power
consumption 60uW in
average. 90LP TSMC.

FIRST
uncompressed WHDI
Chipset (receiver +
transmitter) for
HDTV applications.
90GP TSMC.

FIRST
DuoSense Digitizer
for tablets and
laptops.
90nm Fujitsu.

GSM Backbone
Network Processor.
60M Gates, 24 Mb
SRAM, mixed signal,
FlipChip
at 65LP TSMC.

AAI unique Expertise



Deep-sub-micron (0.18u, 0.13u, 90nm, 65nm, 40nm, 28 nm) System-on-Chip

System architecture in CPU environment (ARM, MIPS, ARC)

Mixed Signal and Full Custom analog designs (A2D, D2A, PMU, LP OSC etc.)

IP integration and verification (ARM, MIPS, USB3.0/2.0, PCI-Ex Gen2, DDR2/3, XAUI, etc.)

Design for test and automatic test pattern generation (ATPG)

Design methodologies for low power applications

Design for manufacturability (DFM): yields, quality, reliability

Advanced assembly techniques: CSP, Flip-Chip, BGA, MCP/SIP

Test program and test hardware development and debug

Logic design flow



Architecture definition, specification

Full RTL design from spec

Integration of complex IPs (AFE & PMU, CPUs, USB, DDR, XAUI etc.)

Design of CPU sub systems (ARM, MIPS, ARC)

System validation and verifications

FPGA design for Asic Emulation

Asic design flow



RTL logic design

IP integration

Synthesis / Physical synthesis

DFT insertion

Formal proof

ATPG

Floor planning: Place and Route

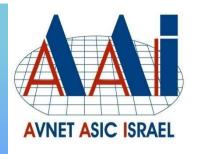
Timing closure

Signal integrity

Physical verification (Extract / DRC / LVS)

Robust Methodologies for Complex SoC Designs, IP integration, Low Power, DSM & DFM Issues

Analog design expertize



Target markets

- Wireless and Consumer Markets
- High speed communication front-end (SerDes, CDR)
- Ultra low power biomedical devices
- Full custom image sensors
- Industrial / Military control
- Custom analog blocks for our digital SoC projects
- High voltage, high current (DMOS) applications

Typical design portfolio

- A/D, D/A converters
 - PLL's, SerDes and CDR's
- Step up/down charge pumps
- Power Management Units LDO, DC2DC, POR, BG, Power Switch, etc.
- Accurate Oscillators with VT Compensation
- High Speed Line drivers
- Electro-optical device drivers
- Analog testing
- Integration of 3rd party IP's (from Chipldea, S3, Cosmic, etc.)
- Low Jitter clocks distribution

Transfer to production and manufacturing services



Tape-Out: GDSII submission to FAB Job View Test program and Hardware dev.

Package definition and design

Silicon manufacturi ng

Wafer probing

Yield tracking

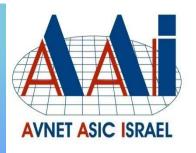
Final testing and correlation to wafer sort

Characteriz ation

Qualificatio n

Solution is custom made to best suite the customer needs

SIP / MCP solutions



System Cost and size saving via advanced packaging options:

- Integrating several dies on single package
- Smaller footprint, less PCB routing, higher performance
- Various integration strategies:
 - Stacked die
 - Side-by-Side
 - Interposer
- 2/4/6 Layer Substrate
- Combining dies of different technologies
- SIP solutions, e.g. Controller + SDRAM + Flash + Power Management
- Combining with AAI ASIC capabilities for complete System in Package, e.g. SoC ASIC + DDR + Analog Driver

Implementation in various package options

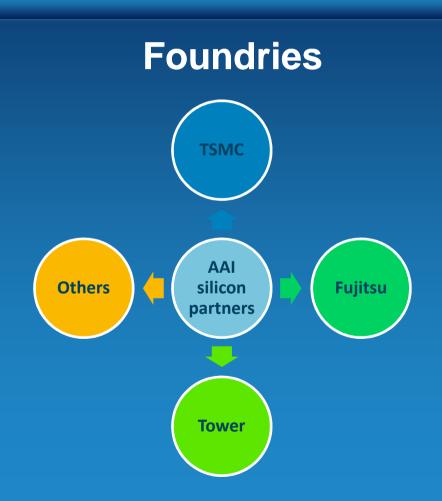
- BGA
- QFN
- Multi-Row QFN
- Flip-Chip
- CSP

Testing and Reliability

Advanced testing techniques to guarantee working module

Manufacturing Vendors







CAD and IP Vendors





Vendor certifications



ARM certified design center (ATAP) **Fujitsu MIPS** approved distributor and design center design center AAI is **ISO** 9001:2000 certified **TSMC** Cadence authorized approved design design center & center **IMEC** partner **Tower** authorized design center

Achievments highlight



- >20 years of continuous activity in the ASIC market as a leading vendor and Design Support Center for High-End ASIC and COT projects
- **>300 first-time-success tape-outs**, most of them complex SoC, integrating many IPs, using various vendors and in various technologies
- **Best reputation over the years** of any ASIC vendor and Design Center in Israel for quality service, on time performance and highest success rate.
- **Samsung** granted AAI team with an Appreciation Plaque for the successful design of Samsung's industry's first WiMax Base-Band chip



AAI's Nadav Ben-Ezer (r.) and Eugene Lyubinsky proudly display the Samsung appreciation plaque.

THANK YOU!